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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte CHUN HSIANG LAI, MENG HUANG LIU,
and TAO CHENG LU

Appeal 2008-006190
Application 09/801,350
Technology Center 2800

Decided:[1] May 28, 2009

Before LINDA M. GAUDETTE, KAREN M. HASTINGS, and MICHAEL P. COLAIANNI, *Administrative Patent Judges*.

HASTINGS, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 1- 4, 13, and 15. We have jurisdiction under 35 U.S.C. § 6(b).

We AFFIRM.

STATEMENT OF THE CASE

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 CFR 1.304, begins to run from the Decided Date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

The invention relates to an electrostatic discharge (ESD) protection circuit. Claim 1, the sole independent claim, is illustrative:

1. An electrostatic discharge (ESD) protection circuit, suitable for use on the I/0 pad, the ESD protection circuit comprising:

a silicon controlled rectifier (SCR) circuit, which comprises *a first connection terminal*, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively *connected to the I/0 pad* and a ground voltage, so as to discharge the electrostatic charges; and

an anti-latch-up circuit, which comprises a *fourth connection terminal*, a fifth connection terminal, and a sixth connection terminal, respectively *coupled to a voltage source*, the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit and thereby prevent latching up of the SCR circuit during normal operation.

(Emphasis added).

The prior art relied upon by the Examiner in the rejection of the appealed claims is:

Ker	5,754,380	May 19, 1998
Quigley	5,781,388	Jul. 14, 1998
Lin	5,982,601	Nov. 9, 1999

The Examiner rejected the claims as follows:

a) claims 1, 3, 4, and 13 under 35 U.S.C. § 102(b) as being anticipated by Lin;

b) claims 1, 3, 4, 13, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Quigley in view of Lin;

c) claim 2 under 35 U.S.C. § 103(a) as being unpatentable over the combined prior art of Quigley, Lin, and Ker, or alternately, over Lin and Ker;

d) claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Lin.

Appellants have not separately argued any of the claims in the first ground of rejection with any reasonable degree of specificity (App. Br. 7-9). Therefore, Appellants have waived any arguments directed to the separate patentability of these claims. *See In re Young,* 927 F.2d 588, 590 (Fed. Cir. 1991); *see also* 37 C.F.R. § 41.37(c)(1)(vii). Also, Appellants have not advanced separate substantive arguments for the Examiner's separate § 103 rejections of dependent claim 2 (*see* Br. 17, 19).

Appellants do present separate arguments regarding dependent claim 15 (Br. 13-15, 17, and 18).

Accordingly, we select independent claim 1 and dependent claim 15 to decide the issues on appeal.

ISSUES ON APPEAL

Have the Appellants shown that the Examiner reversibly erred in rejecting the claims because:

(a) Lin or, alternately, Quigley, does not disclose "a first connection terminal" that is "connected to the I/O pad" as recited in claim 1;

(b) Lin or, alternately, Quigley, does not disclose "a fourth connection terminal" that is "coupled to a voltage source" as recited in claim 1;

(c) Lin, or, alternately, Quigley with Lin, does not render obvious to one of ordinary skill in the art "a RC time delay of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse" as recited in dependent claim 15?

Issues (a) and (b) turn on the broadest reasonable interpretation of claim 1.

PRINCIPLES OF LAW

Claim Construction

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004). This approach is not unfair to applicants, because "before a patent is granted the claims are readily amended as part of the examination process". *Burlington Indus., Inc. v. Quigg*, 822 F.2d 1581, 1583 (Fed. Cir. 1987). It also "serves the public interest by reducing the possibility that claims, finally allowed, will be given broader scope than is justified." *In re Yamamoto*, 740 F.2d 1569, 1571-72 (Fed. Cir. 1984).

Although claims are to be interpreted in light of the specification, limitations from the specification are not to be read into the claims. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993); *see also*, *e.g.*, *In re Zletz*, 893 F.2d 319, 321-22 (Fed. Cir. 1989).

"'[E]ach claim does not necessarily cover every feature disclosed in the specification. When the claim addresses only some of the features disclosed in the specification, it is improper to limit the claim to other, unclaimed features.'" *Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 689 (Fed. Cir. 2008) (quoting *Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1181 (Fed. Cir. 2006)). *See also Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1331 (Fed. Cir. 2004) ("[P]atentees [are]

not required to include within each of their claims all of [the] advantages or features described as significant or important in the written description.").

An applicant seeking a narrower construction must either show why the broader construction is unreasonable or amend the claim to expressly state the scope intended. *In re Morris*, 127 F.3d 1048, 1057 (Fed. Cir. 1997).

Anticipation

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *See Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

However, the law of anticipation does not require that the reference 'teach' what the subject patent (or application) teaches. Assuming that a reference is properly 'prior art,' it is only necessary that the claims, as construed, 'read on' something disclosed in the reference, i.e., all limitations of the claim are found in the reference, or 'fully met' by it. *See Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 772 (Fed. Cir. 1983).

Obviousness

The Supreme Court has instructed that although the teaching, suggestion, and motivation test "captured a helpful insight," an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007).

FINDINGS OF FACTS

Findings of fact throughout this opinion are supported by a preponderance of the evidence.

As found by the Examiner, Lin describes an electrostatic discharge (ESD) protection circuit, including a silicon controlled rectifier circuit (SCR) and an anti-latch-up circuit (Ans. 3-4; e.g., Lin, Figs. 6, 13).

The I/O pad of Lin is connected to a voltage source (Ans. 11, 12; Lin Fig. 6A, *see also*, col. 3, ll. 58-60; *generally* Reply Br., wherein Appellants do not refute the Examiner's finding that "the device would not operate without a voltage source" (Ans. 12)).

As found by the Examiner, Quigley also describes an electrostatic discharge (ESD) protection circuit, including a silicon controlled rectifier circuit (SCR) and an anti-latch-up circuit (Ans. 5, 6; Quigley, Fig. 1), but "does not explicitly state that the voltage rising rate at a node of the anti-latch-up [device] determines whether or not to trigger the SCR circuit" (Ans. 6).

Appellants do not dispute the Examiner's finding that the I/O pad of Quigley is inherently connected to a voltage source (Ans. 13; Quigley, Fig. 1; Reply Br. 5).

One of ordinary skill in the art would have known that that the voltage rising rate at a node of the anti-latch-up device may be used to determine whether or not to trigger the SCR circuit (Lin, Figs. 6, 9, 10, and related text; Ans. 6).

Appellants' Specification describes that in the invention, several I/O pads are coupled to the voltage source through a diode:

> In the invention, *I/0 pads* are coupled to a voltage source Vcc *through a diode*, and the anti-latch-up circuit is coupled between the voltage source and the ground voltage GND. When an ESD event occurs, the diode is forwardly conducted, thereby to trigger the anti-latch-up circuit. *Since the I/0 pads are coupled to the voltage source Vcc through diode, only one anti-latch-up circuit is sufficient to be used for the I/0 pads through the voltage source Vcc*. The layout area is greatly reduced.

(Spec. p. 9, l. 21 to p.10, l. 2; emphasis provided).

Claim 1 does not recite a plurality of I/O pads or a diode.

ANALYSIS

Appellants contend that "the Examiner has misinterpreted that [sic] the pad line of Lin as TWO SEPARATE ELEMENTS" (App. Br. 8) and that Lin shows "the first connection terminal of the SCR circuit and fourth connection terminal of the . . . circuit 61 are respectively connected to the VDD bus or the I/O pad" (Reply Br. 2). Likewise, Appellants' only disagreement with the Examiner's obviousness analysis, based on the combination of Quigley with Lin, is that Quigley fails to show the respective first and fourth connection terminals as claimed because Quigley shows that both of these terminals connect to the same I/O pad, versus the first connection terminal to an I/O pad and the fourth connection terminal to a voltage source (App. Br. 12, Reply Br. 5). Appellants further contend that the advantage of connecting the fourth terminal to the voltage source and the first terminal to the I/O pad is that "only one anti-latch-up circuit is required for several I/O pads, and therefore, the space. . .on the integrated circuit can be effectively reduced" (*e.g.,* App. Br. 9, 13).

We understand Appellants' position to be that the Examiner improperly interpreted the claim language as reading on an embodiment in

which both the SCR circuit and the anti-latch-up circuit are connected to the an I/O pad and coupled to a voltage source. Appellants have the burden of showing that the Examiner's interpretation of the disputed claim terms is unreasonable. For the reasons discussed below, we decline to adopt Appellants' proposed narrow claim interpretation.

The first step in evaluating an anticipation, or obviousness, analysis is to construe the contested limitations correctly to understand their scope and meaning. *See Gechter v. Davidson,* 116 F.3d 1454, 1457 (Fed. Cir. 1997).

Interpreting the claims in light of the Specification, we determine that the claim terms "connected to" and "coupled to" must be read broadly, and are not limited to direct connections. Appellants' claim the sixth terminal is "*directly* connected to" the third terminal (claim 1, emphasis provided), in contrast to the first and fourth terminals being merely "connected to" or "coupled to" the I/O pad and voltage source, respectively - plainly indicating that the connections in dispute do not need to be direct connections. Correspondingly, the Specification describes coupling the I/O pad 100 to the voltage source Vcc *through* the diode 108. (Spec. 10:21-23.) The Specification also describes the fourth connection terminal as "coupled to" the voltage source, rather than directly connected. (Spec. 11:3-5.) In addition, while we interpret claim 1 as requiring coupling of the fourth terminal to a voltage source, we see no basis in the claim language or Specification which warrants interpretation of claim 1 as *precluding* connection of the anti-latch-up circuit to the I/O pad.

Accordingly, we find no basis in the language of claim 1 or in the disclosure in the Specification on which to read the disputed language in the narrow sense urged by Appellants. In this regard, we note that our

reviewing court has repeatedly cautioned against limiting otherwise broad claim language to cover a specifically disclosed embodiment in the manner proposed by Appellants (Reply Br. 5 (arguing a claim interpretation based on Specification Figure 4)). *See, e.g., Howmedica Osteonics Corp. v. Wright Medical Tech., Inc.,* 540 F.3d 1337, 1345 (Fed. Cir. 2008) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc)).[2]

Furthermore, the Specification describes that the advantage urged by Appellants as resulting from the claimed first and fourth connections actually results from having several "I/O pads coupled to the voltage source Vcc through [a] diode" (Spec. p. 9, l. 21 to p. 10, l. 2) . Claim 1 is not limited to such a configuration.

The plain meaning and reading of the claimed circuit connections at issue reasonably encompasses the circuit described in Lin or the combination of Quigley and Lin as aptly explained by the Examiner. In other words, the claim language does not distinguish from the (first and fourth) connection terminals of Lin, or Quigley that may both be connected to an I/O pad that in turn is inherently connected to a voltage source.

Appellants have not provided any credible evidence or reasoning to refute the Examiner's position that the I/O pads of the applied prior art circuits must have a voltage source, such that when terminals of the SCR

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[2] In fact, Appellants themselves acknowledge that their proposed claim interpretation is merely implied. (Reply Br. 5 ("[T]he fact that the [sic] claim 1 recites that 'the first connection terminal of the SCR circuit is connected to the I/O pad and the fourth connection terminal of the anti-latch-up circuit is connected to a voltage source' would imply that the voltage source is other than the I/O pad, and that the I/0 pad and the voltage source are two separate elements (this is well supported in FIG. 4 of the present invention).").)

and anti-latch-up devices are connected to an I/O pad, they are also coupled to a voltage source, as claimed in claim 1. Therefore, we determine that Appellants have not identified reversible error in the Examiner's finding that claim 1 is anticipated by Lin or that claim 1 is obvious in view of Quigley and Lin.

The Obviousness Rejections of Dependent Claim 15

Appellants contend that Lin does not teach or suggest that the anti-latch up circuit has a RC time delay as claimed in claim 15 (i.e., "smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse") (App. Br. 18). Appellants contend that Lin teaches an RC delay time smaller than the ESD voltage ramp rate and therefor teaches away from the claimed invention (*id.*). Likewise, Appellants contend that Quigley also teaches away from the feature of claim 15 (App. Br. 14).

We do not find these arguments persuasive of error in the Examiner's rejections. A reference "teaches away" when it suggests that the developments flowing from its disclosures are unlikely to produce the objective of the Appellants' invention. *See In re Gurley,* 27 F.3d 551, 553 (Fed. Cir. 1994). Certainly, skill in the art is presumed, and as the Examiner explained, one of ordinary skill would have been motivated to use a RC time delay as recited in claim 15 since:

> Lin explicitly teaches that using an RC relay time of the RC anti-latch-up circuit larger than the voltage rising phase of the ESD transient, would more easily trigger the SCR [silicon controlled rectifier circuit] during an ESD event (column 4, lines 26-32). Lin further teaches that using an RC relay time of the RC anti-latch-up circuit less (smaller) than the powering up

> transient, would prevent the SCR from being triggered during normal operation or powering up. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit [which] is smaller than a voltage rising time of an IC power and greater than a voltage rising time of an ESD pulse, as taught by Lin, in Quigley, as claimed.
>
> (Ans. 14).

Appellants have not persuasively explained why the Examiner erred in determining that Lin alone provides a basis for the obviousness of the claimed feature since "[a]n artisan would also be motivated to use an RC relay time of the RC anti-latch-up circuit less (smaller) than the powering up transient, so that the SCR does not trigger during normal operation or powering up." (Ans. 15). *See also KSR,* 550 U.S. 398 at 421 (one of ordinary skill in the art is "also a person of ordinary creativity, not an automaton").

Accordingly, Appellants have not shown reversible error in the Examiner's conclusion of obviousness as to dependent claim 15, based on either Lin alone or the combination of Quigley and Lin. We therefore sustain the § 103 rejections advanced by the Examiner based on Lin, or the combined prior art of Quigley and Lin, for claim 15 in this appeal.

CONCLUSION

Appellants have not shown reversible error in the Examiner's finding that Lin, or alternately Quigley, includes first and fourth connection terminals respectively connected to an I/O pad and voltage source as claimed.

Appellants have also not shown that Lin, or alternately Quigley with Lin does not render "a RC time delay" as recited in dependent claim 15 obvious to one of ordinary skill in the art.

It follows that we sustain the § 102 rejection of claims 1, 3, 4, and 13 being anticipated by Lin. We also sustain all of the § 103 rejections advanced by the Examiner in this appeal.

ORDER

The Primary Examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

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